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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,735	05/11/2001	Mototsugu Okushima	NE212-US	4991

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EXAMINER

NADAV, ORI

ART UNIT PAPER NUMBER

2811

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/852,735

Applicant(s)

OKUSHIMA, MOTOTSUGU

Examiner

Ori Nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 73-75 and 77-85 is/are pending in the application.
- 4a) Of the above claim(s) 80-85 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 73-75 and 77-79 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 73-75 and 77-79 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification, as filed, for a vertical bipolar transistor being formed on a semiconductor substrate for discharging accumulated electric charge from a surface layer of said semiconductor substrate towards depth direction of said semiconductor substrate, as recited in claim 73.

Claims 73-75 and 77-79 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of vertical bipolar transistor leads out collector electrodes through a collector-connection well, as recited in

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claim 73, are unclear as to how collector electrodes, which are located above the substrate, can be led out through a collector-connection well which is located in the substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 73-75 and 77-79, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwai et al. (5,648,676) in view of Li et al. (5,623,387).

Iwai et al. teach in figure 2a and related text an ESD protection device for protecting a transistor from an overvoltage, said ESD protection element comprising:

a vertical bipolar transistor 14 being formed on a semiconductor substrate 19 for discharging accumulated electric charge from a surface layer of said semiconductor substrate towards depth direction of said semiconductor substrate, wherein

said vertical bipolar transistor leads out collector electrodes through a collector-connection region 20a and

said vertical bipolar transistor has a collector 20a and a base 29a formed in a same region.

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Iwai et al. do not teach an ESD protection device connected between a CMOS transistor and a pad for protecting said CMOS transistor from an overvoltage applied to said pad, a collector-connection region being a well, and the composition of a trigger device used for switching said bipolar transistor of said ESD protection device.

Li et al. teach in figure 4a an ESD protection device connected between a CMOS transistor T3, T4 and a pad 101 for protecting said CMOS transistor from an over-voltage applied to said pad, and

a trigger device for switching said bipolar transistor of said ESD protection device using an application of an over-voltage as a trigger, wherein said trigger device comprises:

a diode D124 having, in a joined state, a first conductive region formed simultaneously with said base of said vertical bipolar transistor on a surface of a semiconductor substrate and a second conductive region simultaneously formed with an emitter on a surface of said semiconductor substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Iwai et al.'s ESD protection device to protect a CMOS transistor from an over-voltage applied to a pad, to form the collector-connection region as a well, and to use a trigger device for switching said bipolar transistor of said ESD protection device, as taught by Li et al., in Iwai et al.'s device, in order to use the ESD device in an application which requires protection to a CMOS transistor from an over-voltage applied to a pad, in order to improve the electrical isolation of the device by

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forming the collector-connection region in a conventional method (as a well), and in order to prevent excess build-up, respectively.

Regarding the process limitations recited in claims 73 and 75 ("forming the collector and the base by using the same mask", and "a first conductive region formed simultaneously with said base of said vertical bipolar transistor on a surface of a semiconductor substrate and a second conductive region simultaneously formed with an emitter on a surface of said first conductive region"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding the claimed limitations of a trigger device used for switching said bipolar transistor of said ESD protection device by an application of an over-voltage as a trigger, these intended use recitations must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed

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invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. Note that applicant uses a diode as a trigger device, and Li et al. also teach a diode. Therefore, Li et al.'s diode can also be used as a trigger device.

Regarding claim 74, Li et al. teach an ESD protection device comprising plural of bipolar transistors adjacent to each other. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use plural of vertical bipolar transistors adjacent to each other in Iwai et al.'s ESD protection device in order to provide better protection to the internal circuit.

Regarding claim 77, Li et al. teach in the diode of said trigger device; said first conductive region forms an anode and said second conductive region forms cathode; said semiconductor substrate is of a first conductive type and said anode and said cathode are insulated in a region of a second conductive type that is simultaneously formed with said collector of said transistor.

Regarding claims 78 and 79, in the trigger device of prior art's device, the anode is connected with said base of said vertical bipolar transistor and said cathode is connected with said collector said vertical bipolar transistor since all the circuit elements are electrically connected to each other, wherein Iwai et al. teach in figure 5a the base

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10a of the vertical bipolar transistor is connected with a ground terminal through a resistor 61.

Response to Arguments

Applicant argues that there is support in the specification, as filed, for a vertical bipolar transistor being formed on a semiconductor substrate for discharging accumulated electric charge from a surface layer of said semiconductor substrate towards depth direction of said semiconductor substrate, as recited in claim 73, because the specification describes on page 16, lines 1-6 that the electric charge is released in the longitudinal direction of the silicon substrate, and as a result, electric current concentration can be prevented and a high ESD withstand level can be obtained.

Although the specification describes on page 16, lines 1-6 that the electric charge is released in the longitudinal direction of the silicon substrate, and as a result, electric current concentration can be prevented and a high ESD withstand level can be obtained, this passage does not provide support for a vertical bipolar transistor formed on a semiconductor substrate for discharging accumulated electric charge from a surface layer of said semiconductor substrate towards depth direction of said semiconductor substrate, as recited in claim 73.

Applicant argues that the claimed limitations of vertical bipolar transistor leads out collector electrodes through a collector-connection well, as recited in claim 73, are

clear, because the specification describes on page 16, lines 1-6 that the electric charge is released in the longitudinal direction of the silicon substrate, and thus, the collector electrodes are led out through collector-connection from a surface of the substrate through the substrate towards the depth direction of the semiconductor substrate, as recited.

Although the specification describes on page 16, lines 1-6 that the electric charge is released in the longitudinal direction of the silicon substrate, this passage does not clarify the claimed limitations of vertical bipolar transistor leads out collector electrodes through a collector-connection well, as recited in claim 73. These limitations are unclear since an artisan can not ascertain how collector electrodes, which are located above the substrate, can be led out through a collector-connection well which is located in the substrate.

Applicant argues since diode Z124 of Li et al. is located between the base region (beneath field oxide 306b) and collector 305, and the base and collector of Iwai et al.'s device are short-circuited together, then It is not apparent where the diode of Li et al. would be used the short-circuited device of Iwai et al.

Diode Z124 of Li et al. do not need to be the trigger device. Diode D124, or any other diode in the circuit can be used as the trigger device. Diode D124, for example, is not connected between the base and the collector. Therefore, the diode of Li et al. can be used in Iwai et al.'s device.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized flourish at the end.

O.N.
10/26/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800